AMENDMENT TO THE CLAIMS

 (currently amended) A method for making a programmable resistance memory element, comprising:

providing a conductive material;

forming a sidewall spacer over said conductive material;

forming a second layer over said conductive material;

forming a sidewall surface in said second layer;

forming a third layer over said sidewall surface;

removing a portion of said third layer, a remaining

portion of said third layer being a sidewall spacer;

using said sidewall spacer as a mask, removing a portion of said conductive material to form a raised portion of said conductive material under said spacer; and

forming a programmable resistance material in electrical contact with said raised portion.

- 2. (currently amended) The method of claim 1, wherein said removing said conductive material step comprises etching said conductive material.
- 3. (original) The method of claim 2, wherein said etching step comprises anisotropically etching said conductive material.
- 4. (original) The method of claim 2, wherein said etching step comprises isotropically etching said conductive material.

Claim 5 Canceled

6. (currently amended) The method of claim $\frac{5}{2}$, further comprising:

before forming said second layer, forming a first layer over said conductive material and then—forming said second layer over said first layer, said second layer then being formed over said first layer.

- 7. (original) The method of claim 6, further comprising: after removing said portion of said third layer, removing said second layer; and removing a portion of said first layer.
- 8. (currently amended) The method of claim $\frac{5}{2}$, wherein said removing said portion of said third layer step comprises anisotropically etching said third layer.
- 9. (original) The method of claim 6, wherein said removing said portion of said first layer comprises anisotropically etching said first layer.
- 10. (original) The method of claim 6, wherein said first and third layers are oxides.

- 11. (currently amended) The method of claim $\frac{5}{2}$, wherein said second layer is polysilicon.
- 12. (original) The method of claim 6, wherein said first and third layers are nitrides.
- 13. (currently amended) The method of claim $\frac{5}{2}$, wherein said second layer is an oxide.
- 14. (currently amended) The method of claim 1, wherein said sidewall spacer third layer comprises a material selected from the group consisting of dielectric, semiconductor, and conductor.
- 15. (currently amended) The method of claim 1, wherein said sidewall spacer third layer comprises a material selected from the group consisting of oxide and nitride.
- 16. (currently amended) The method of claim 1, wherein said eidewall spacer third layer comprises polysilicon.
- 17. (original) The method of claim 1, wherein said programmable resistance material comprises a phase change material.

- 18. (original) The method of claim 1, wherein said programmable resistance material comprises a chalcogen element.
- 19. (new) The method of claim 1, further comprising:
 after removing said portion of said third layer and
 before removing said portion of said conductive material,
 removing said second layer.
- 20. (new) The method of claim 1, wherein said forming said third layer comprises conformally depositing said third layer.
- 21. (new) The method of claim 8, wherein said forming said third layer comprises conformally depositing said third layer.
- 22. (new) The method of claim 1, wherein said programmable resistance material is formed in electrical contact with a top surface of said raised portion.
- 23. (new) A method for making a programmable resistance memory element, comprising:

providing a conductive material;

forming a second layer over said conductive material;

forming a sidewall surface in said second layer;

conformally depositing a third layer over said sidewall

surface;

anisotropically etching said third layer;

using said third layer as a mask, removing a portion of said conductive material to form a raised portion of said conductive material under said third layer; and

forming a programmable resistance material in electrical contact with said raised portion.

- 24. (new) The method of claim 23, wherein said removing said conductive material step comprises etching said conductive material.
- 25. (new) The method of claim 24, wherein said etching step comprises anisotropically etching said conductive material.
- 26. (new) The method of claim 24, wherein said etching step comprises isotropically etching said conductive material.
- 27. (new) The method of claim 23, further comprising: before forming said second layer, forming a first layer over said conductive material, said second layer then being formed over said first layer.
- 28. (new) The method of claim 27, further comprising:

 after removing said portion of said third layer,
 removing said second layer; and
 removing a portion of said first layer.

- 29. (new) The method of claim 28, wherein said removing said portion of said first layer comprises anisotropically etching said first layer.
- 30. (new) The method of claim 23, wherein said third layer comprises a material selected from the group consisting of oxide and nitride.
- 31. (new) The method of claim 23, wherein said third layer comprises polysilicon.
- 32. (new) The method of claim 23, wherein said programmable resistance material comprises a phase change material.
- 33. (new) The method of claim 23, wherein said programmable resistance material comprises a chalcogen element.